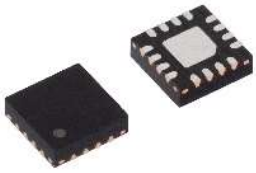
MITSUMI

Nov. 2024 , Rev.2

Two-channel 16-, 14-, and 12-bit SAR ADC
MM4027A16, MM4027A14, MM4027A12 data sheet

DESCRIPTION



MM4027A16, MM4027A14 and MM4027A12 is a successive approximation type of AD converter IC, which up to 750 ksps.

The analog signal is a pseudo-differential input, enabling simultaneous measurement of two analog signals.

Communication with an external digital host is performed by SPI serial communication.

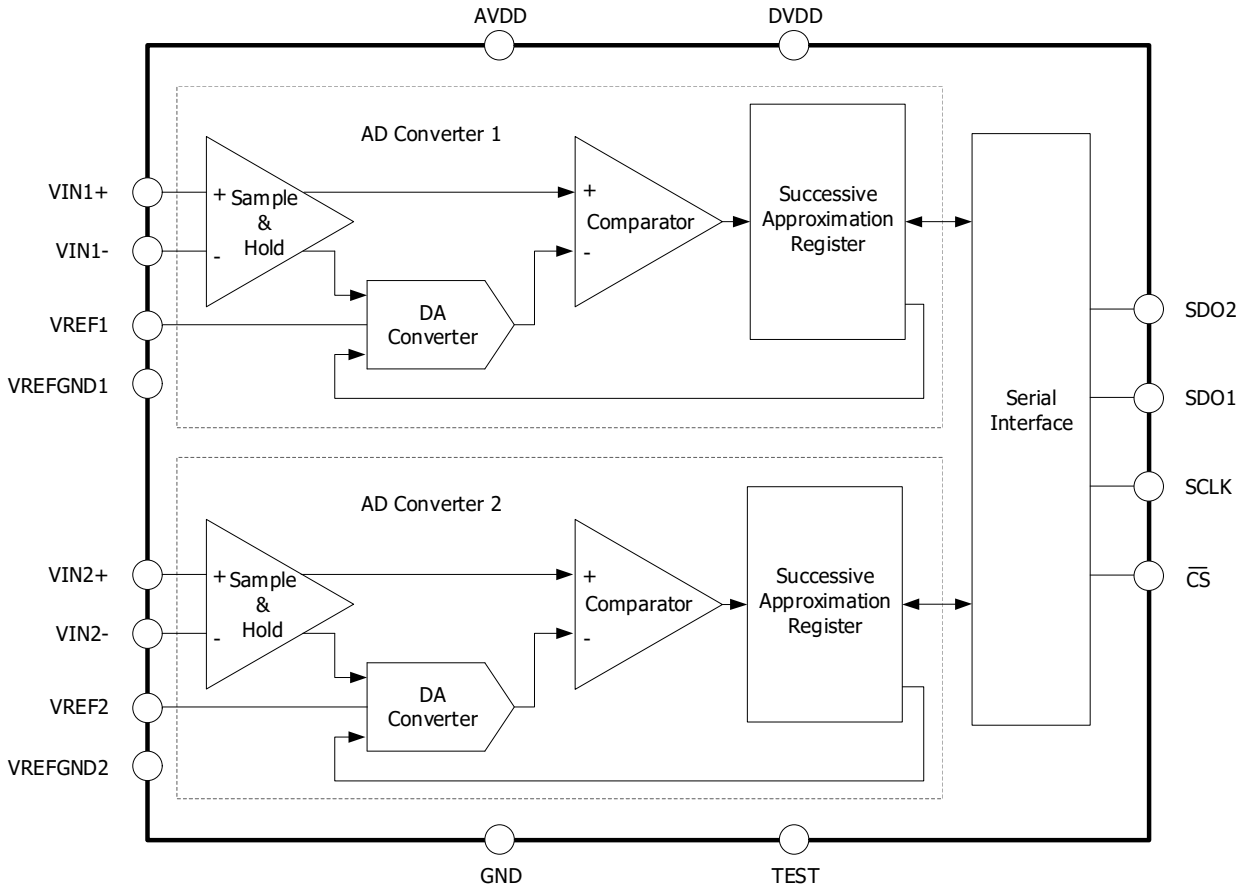
Each device has different resolutions: 16-bit for A16, 14-bit for A14, and 12-bit for A12.

FEATURES

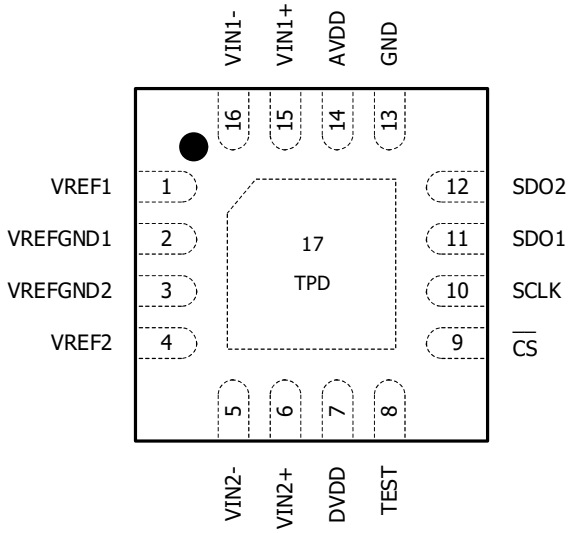
- Lineup of three types of resolution : 16-, 14-, and 12-bit
- No Missing Codes
- Sampling Rate : 750 ksps
- Pseudo differential analog inputs
- Two-channel simultaneous sampling
- DC Performance
  - MM4027A16 : ±2.5 LSB Max. INL
  - MM4027A14 : ±1.5 LSB Max. INL
  - MM4027A12 : ±1 LSB Max. INL
- AC Performance
  - MM4027A16 : 85 dB SNR, -96 dB THD
  - MM4027A14 : 81.5 dB SNR, -90 dB THD
  - MM4027A12 : 73 dB SNR, -90 dB THD
- SPI compatible serial communication
- Temperature Range : -40°C to +125°C

Contents

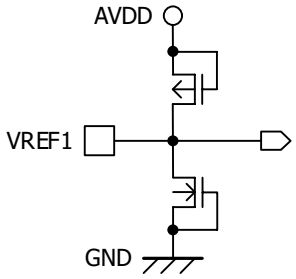
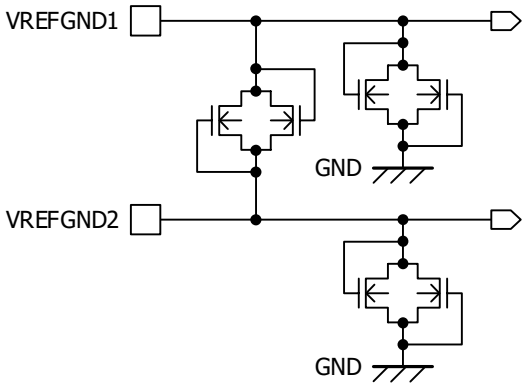
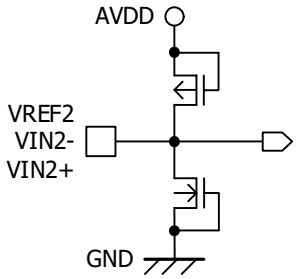
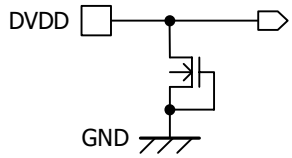
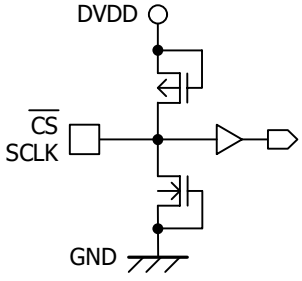
BLOCK DIAGRAM



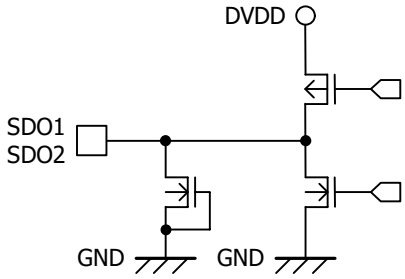
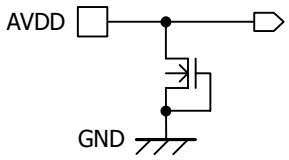
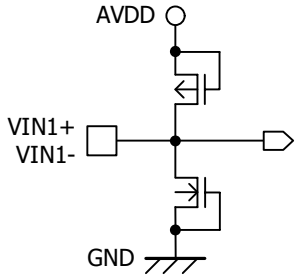
PIN CONFIGURATION



TERMINAL EXPLANATIONS

No.	Pin Name	Type	Internal Equivalent Circuit	Function
1	VREF1	Input		Reference voltage input for ADC1
2	VREFGND1	Supply		Reference voltage GND for ADC1
3	VREFGND2	Supply		Reference voltage GND for ADC2
4	VREF2	Input		Reference voltage input for ADC2
5	VIN2-	Input		Minus analog input for ADC2
6	VIN2+	Input		Plus analog input for ADC2
7	DVDD	Supply		Power supply for digital I/O
8	TEST	Supply	-	Test Pin * Be sure to connect to GND.
9	$\overline{CS}$	Input		Chip select input
10	SCLK	Input		Serial communication clock input

TERMINAL EXPLANATIONS

No.	Pin Name	Type	Internal Equivalent Circuit	Function
11	SDO1	Output		Serial communication data output for ADC1
12	SDO2	Output		Serial communication data output for ADC2
13	GND	Supply	-	Ground
14	AVDD	Supply		Power supply for ADC
15	VIN1+	Input		Plus analog input for ADC1
16	VIN1-	Input		Minus analog input for ADC1
17	TPD	Supply	-	Thermal pad * Be sure to connect to GND.

ABSOLUTE MAXIMUM RATINGS

Unless otherwise specified
Ta=25°C

Item	Symbol	Min.	Max.	Unit
Supply voltage	VDD_{abx}	-0.3	7.0	V
Analog input voltage (note[1])	V_{AINabx}	GND – 0.3	AVDD + 0.3	V
Digital input voltage (note[2])	V_{DINabx}	GND – 0.3	DVDD + 0.3	V
Ground voltage difference (|VREFGND1,2 - GND|)	$\|GND_d\|$	0.3		V
Storage temperature	T_{stg}	-65	150	°C
Power dissipation(On board)	P_d	2.7		W

note[1] : VIN1+, VIN1-, VREF1, VIN2+, VIN2-, VREF2
note[2] : CS, SCLK, SDO1, SDO2

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified
Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit
Operating ambient temperature	T_{op}	-40	-	125	°C
AVDD operating voltage	$AVDD_{op}$	4.5	5	5.5	V
DVDD operating voltage	$DVDD_{op}$	1.65	3.3	AVDD	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified

Min. and max. specifications : T_a = –40°C to 125°C, AVDD = 5 V, VREF1 = VREF2 = V_{ref} = 2.5 V, Sampling rate (f_{sample}) = 750 ksps

Typ. values : T_a = 25°C, AVDD = 5 V, and DVDD = 3.3 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.
Power supply						
Analog supply current (operational)	I_{avop}	AVDD = 5 V, f_{sample} = 750 ksps	-	8.0	9.0	mA
Analog supply current (static)	I_{avst}	AVDD = 5 V, $\overline{CS}$ =H	-	5.0	7.0	mA
Digital supply current	I_{dv}	DVDD = 3.3 V, f_{sample} = 750 ksps	-	0.5	-	mA
Analog input						
Full-scale input range (VIN*+ - VIN*-)	FSR	(note[3])	-V_{ref}	-	V_{ref}	V
Absolute input voltage (+) (VIN*+ - VREFGND*)	V_{in+}	(note[3])	0.0	-	2 × V_{ref}	V
Absolute input voltage (-) (VIN*- - VREFGND*)	V_{in-}	(note[3])	V_{ref} – 0.1	V_{ref}	V_{ref} + 0.1	V
Input capacitance (note[4])	C_{ain}	Sample mode	-	40	-	pF
		Hold mode	-	4	-	pF
Input leakage current	I_{ain}		-	1.5	-	nA
Reference voltage input						
Reference input voltage	V_{ref}		2.25	2.5	AVDD / 2	V
Current drain	I_{ref}	Input current	-	300	-	uA
	I_{refl}	Leakage current	-	-	1	uA

note[3] : AVDD and VREF* must satisfy AVDD ≥ 2 × VREF* for maximum dynamic range.
VIN*+, VIN*-, VREFGND* and VREF* denotes the following, respectively.
VIN*+ = VIN1+ or VIN2+
VIN*- = VIN1- or VIN2-
VREFGND* = VREFGND1 or VREFGND2
VREF* = VREF1 or VREF2

note[4] : Specified by design

ELECTRICAL CHARACTERISTICS

Unless otherwise specified

Min. and max. specifications : T_a = –40°C to 125°C, AVDD = 5 V, VREF1 = VREF2 = V_{ref} = 2.5 V, Sampling rate (f_{sample}) = 750 ksps

Typ. values : T_a = 25°C, AVDD = 5 V, and DVDD = 3.3 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.
Sampling dynamics						
Sampling rate	f_{sample}		-	-	750	ksps
Aperture delay (note[5])	t_{ap}		-	8	-	ns
	t_{apm}	Aperture delay deference between ADC1 and ADC2.	-	40	-	ps
Aperture jitter (note[5])	t_{apj}		-	10	-	ps
Clock frequency	f_{clk}		-	-	24	MHz
Digital input						
High level input voltage (note[5])	V_{ih}		0.7 × DVDD	-	DVDD + 0.3	V
Low level input voltage (note[5])	V_{il1}	DVDD ≧ 2 V	-0.30	-	0.3 × DVDD	V
	V_{il2}	DVDD < 2 V	-0.30	-	0.2 × DVDD	V
Digital output						
High level output voltage (note[5])	V_{oh}	I_{oh} = 500 µA, source	0.8 × DVDD	-	DVDD	V
Low level output voltage (note[5])	V_{ol}	I_{ol} = 500 µA, sink	0	-	0.2 × DVDD	V

note[5] : Specified by design

ELECTRICAL CHARACTERISTICS

Unless otherwise specified

Min. and max. specifications : T_a = –40°C to 125°C, AVDD = 5 V, VREF1 = VREF2 = V_{ref} = 2.5 V, Sampling rate (f_{sample}) = 750 ksps

Typ. values : T_a = 25°C, AVDD = 5 V, and DVDD = 3.3 V

Item	Symbol	Condition	MM4027A16			MM4027A14			MM4027A12			Unit.
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Resolution												
Resolution	RESO		-	-	16	-	-	14	-	-	12	Bits
DC accuracy												
Integral nonlinearity	INL		-2.5	±1	2.5	-1.5	±0.8	1.5	-1	±0.5	1	LSB (note[6])
Differential nonlinearity	DNL		-0.99	±0.7	2	-0.99	±0.7	1	-0.99	±0.4	1	LSB
Input offset error	V_{of}		-1	±0.25	1	-1	±0.25	1	-2	±0.75	2	mV
	V_{ofm}	Offset error deference between ADC1 and ADC2.	-1	±0.25	1	-1	±0.25	1	-2	±0.75	2	mV
Input offset thermal drift (note[7])	$\lvert dV_{of}/dt \rvert$		-	1	-	-	1	-	-	1	-	uV/°C
Gain error	G_{err}	Refers to the voltage of VREF1 and VREF2.	-0.1	±0.05	0.1	-0.1	±0.05	0.1	-0.1	±0.05	0.1	%
	G_{errm}	Gain error deference between ADC1 and ADC2.	-0.1	±0.05	0.1	-0.1	±0.05	0.1	-0.1	±0.05	0.1	%
Gain error thermal drift (note[7])	$\lvert G_{err}/dt \rvert$	Refers to the voltage of VREF1 and VREF2.	-	1	-	-	1	-	-	1	-	ppm/°C
Common mode rejection ratio	CMRR	Signals of DC to 20kHz are input to ADC1 and ADC2.	-	74	-	-	74	-	-	74	-	dB

note[6] : For VREF=2.5V, the ideal value of 1 LSB is as follows.

MM4027A16 : $2 \times VREF / 2^{16} \fallingdotseq 76$ uV

MM4027A14 : $2 \times VREF / 2^{14} \fallingdotseq 305$ uV

MM4027A12 : $2 \times VREF / 2^{12} \fallingdotseq 1.22$ mV

note[7] : Specified by design

ELECTRICAL CHARACTERISTICS

Unless otherwise specified

Min. and max. specifications : T_a = –40°C to 125°C, AVDD = 5 V, VREF1 = VREF2 = V_{ref} = 2.5 V, Sampling rate (f_{sample}) = 750 ksps

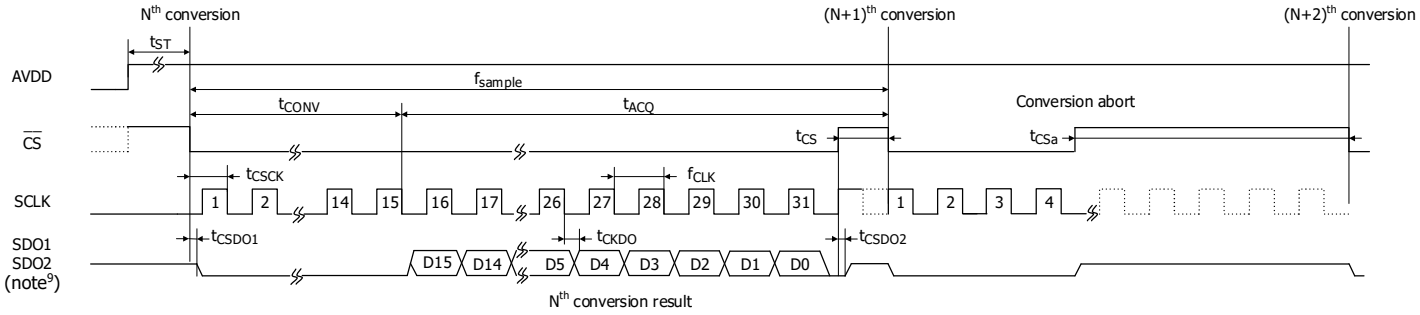
Typ. values : T_a = 25°C, AVDD = 5 V, and DVDD = 3.3 V

Item	Symbol	Condition	MM4027A16			MM4027A14			MM4027A12			Unit.
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
AC accuracy												
Signal to (noise + distortion) ratio	SINAD	-0.5 dB [full scale] at 20 kHz input	83.5	84.7	-	79	81	-	71.5	72.9	-	dB
		-0.5 dB [full scale] at 100 kHz input	-	83.7	-	-	81	-	-	72.9	-	dB
		-0.5 dB [full scale] at 250 kHz input	-	83	-	-	79.9	-	-	72.5	-	dB
Signal to noise ratio	SNR	-0.5 dB [full scale] at 20 kHz input	84	85	-	79.5	81.5	-	72	73	-	dB
		-0.5 dB [full scale] at 100 kHz input	-	84.8	-	-	81.5	-	-	73	-	dB
		-0.5 dB [full scale] at 250 kHz input	-	84	-	-	81	-	-	73	-	dB
Total harmonic distortion	THD	-0.5 dB [full scale] at 20 kHz input	-	-96	-	-	-90	-	-	-90	-	dB
		-0.5 dB [full scale] at 100 kHz input	-	-90	-	-	-90	-	-	-90	-	dB
		-0.5 dB [full scale] at 250 kHz input	-	-90	-	-	-86	-	-	-82	-	dB
Spurious free dynamic range	SFDR	-0.5 dB [full scale] at 20 kHz input	-	96	-	-	90	-	-	90	-	dB
		-0.5 dB [full scale] at 100 kHz input	-	90	-	-	90	-	-	90	-	dB
		-0.5 dB [full scale] at 250 kHz input	-	90	-	-	86	-	-	82	-	dB
Isolation between ADC1 and ADC2	ISO_{12}	f_{IN} = 15 kHz, f_{NOISE} = 25 kHz	-	-90	-	-	-90	-	-	-85	-	dB
Full power bandwidth	BW_{FP}	-3 dB	-	25	-	-	25	-	-	25	-	MHz
		-0.1 dB	-	5	-	-	5	-	-	5	-	MHz

TIMING CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.
Sampling rate	f_{sample}		-	-	750	ksps
Clock frequency	f_{clk}		-	-	24	MHz
Clock duty	Duty		40	-	60	%
Standby time after power-on	t_{ST}		-	0.5	-	ms
Conversion time	t_{CONV}		-	-	15	clock cycles
Acquisition time	t_{ACQ}	MM4027A16, f_{clk}=24MHz	120	-	-	ns
		MM4027A14, f_{clk}=24MHz	100	-	-	ns
		MM4027A12, f_{clk}=24MHz	70	-	-	ns
CS high time	t_{CS}		20	-	-	ns
CS high time after conversion abort	t_{CSa}	MM4027A16	120	-	-	ns
		MM4027A14	100	-	-	ns
		MM4027A12	70	-	-	ns
SCLK setup time	t_{CSCK}		15	-	-	ns
SDO delay time from SCLK falling edge (note[8])	t_{CKDO}	1.65 V < DVDD ≦ 2.3 V	3	-	TBD	ns
		2.3 V < DVDD ≦ 2.7 V	3	-	22	ns
		2.7V < DVDD	3	-	20	ns
SDO tristate delay time 1	t_{CSDO1}		-	-	12	ns
SDO tristate delay time 2	t_{CSDO2}		-	-	10	ns

note[8] : With 20 pF load, the fall is defined at 20% DVDD and the rise at 80% DVDD.



note[9] : SDO data is captured at the falling edge of SCLK.

Figure-1. Analog to digital conversion timing diagram

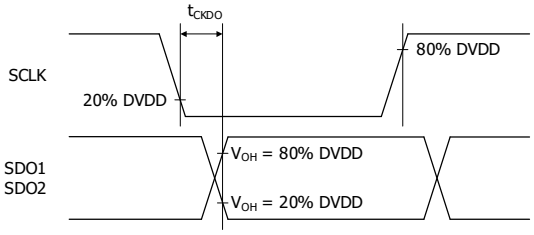


Figure- 2. Voltage level of t_{CKDO} measurement

DETAILED DESCRIPTION

Overview

MM4027 series is a successive approximation type AD converter IC, with up to 750 ksps that can measure two analog signals simultaneously. The analog signal is a pseudo-differential input, and communication with an external digital host is performed by SPI serial communication.

The lineup contains 16-bit resolution MM4027A16, 14-bit MM4027A14, and 12-bit MM4027A12.

Analog to digital conversion

Figure-3 shows the timing diagram. AD conversion of MM4027 series starts from the $\overline{CS}$ falling edge and SCLK digitally converts the sampled analog value between 14 clocks. SDO1 and SDO2 readings are "0" during this transformation.

The sample-and-hold circuit returns to sample mode on the 14th SCLK falling edge, and the MSBs of ADC1 and ADC2 are output on the 15th SCLK falling edge to SDO1 and SDO2, respectively. Since the conversion result is output sequentially from the subsequent falling edge, a SCLK falling edge with a minimum of 14 + resolution is required between the $\overline{CS}$ falling edge and the $\overline{CS}$ rising edge to perform AD conversion. For MM4027A16, LSB are outputted at the 30th SCLK falling edge.

If the $\overline{CS}$ low continues after the LSB is output, SDO1 and SDO2 output "0" until the $\overline{CS}$ rising edge. The conversion frame ends at the $\overline{CS}$ rising edge, and SDO1 and SDO2 are Hi-Z.

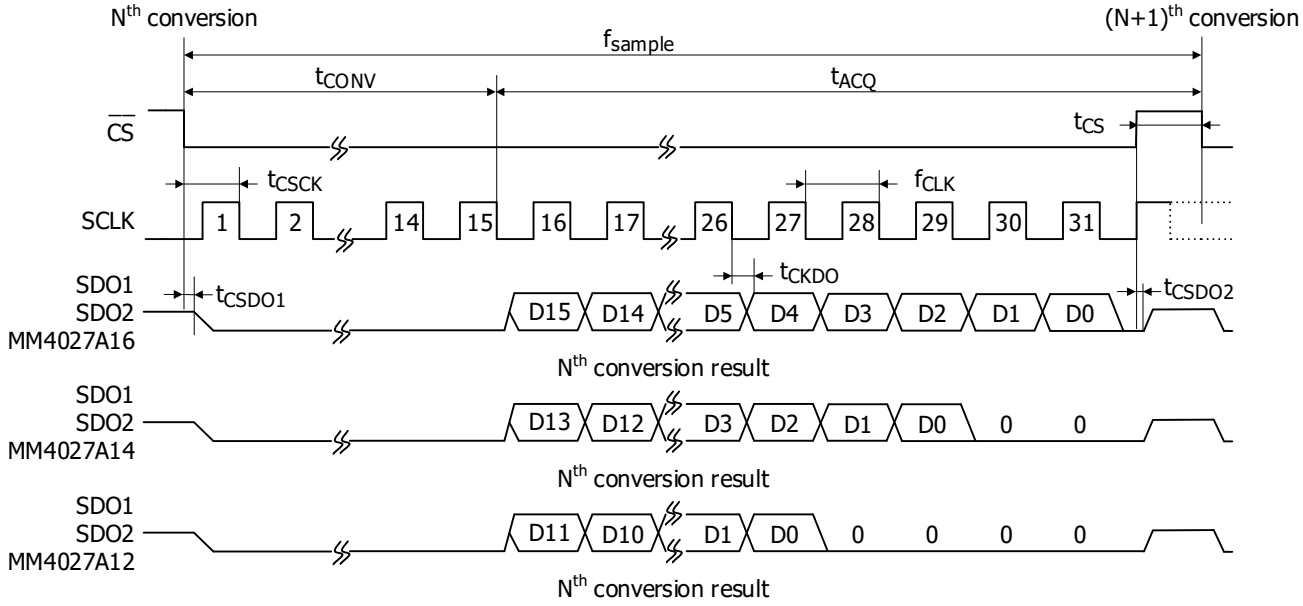


Figure-3. Analog to digital conversion timing

DETAILED DESCRIPTION

Short cycle read

Figure-4 shows the timing diagram of short cycle read. The sampled input analog value is output from the MSB to SDO1 and SDO2 sequentially from the 15th SCLK falling edge after SCLK completes the digital conversion between 14 clocks, but if $\overline{CS}$ is made high prior to the LSB output, the output of the subsequent SDO1 and SDO2 is Hi-Z.

The output data from SDO1 and SDO2 before the CS is made high is valid. In some cases, CS high time after conversion abort (t_{CSa}) to set aside enough time to collect analog signals until the conversion frame.

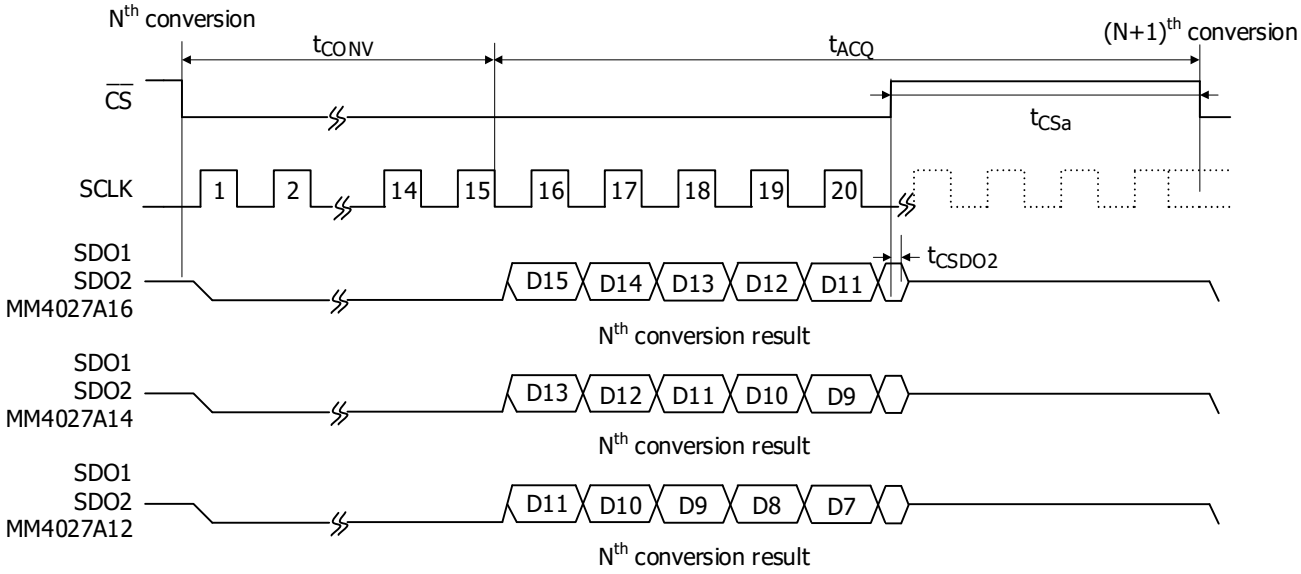


Figure-4. Short cycle read

Conversion abort, Reconversion, Power-on

As shown in Figure-5, if $\overline{CS}$ is set to high prior to the 14th SCLK falling, conversion is interrupted and sampling of the next analog input signal begins. $\overline{CS}$ must reserve the $\overline{CS}$ high time after conversion abort (t_{CSa}) in order to secure the collection time until the next conversion frame.

When the power is turned on, the standby time after power-on (t_{ST}) must be secured after the power is turned on. If the waiting time is insufficient, normal data may not be output. In this case, discard the data for the first time before use.

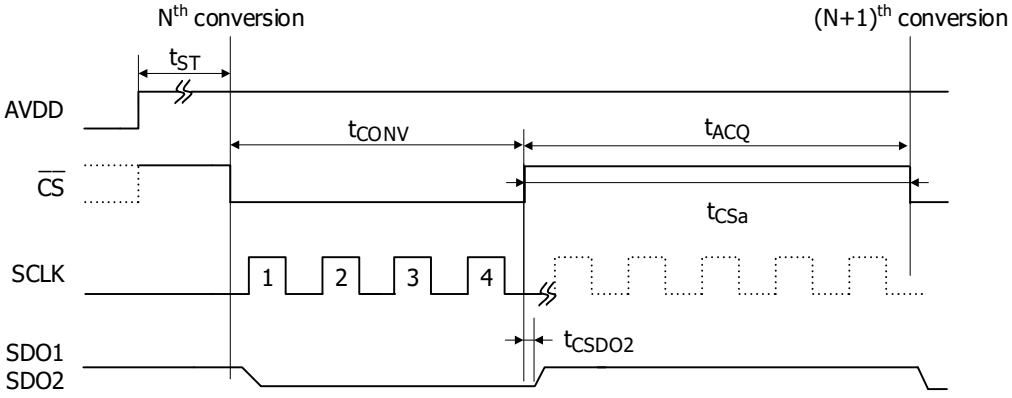


Figure-5. Conversion abort

DETAILED DESCRIPTION

Analog input

MM4027 series supports pseudo-differential input of analog signals. There are two channels of analog input and simultaneous sampling is possible.

Figure-6 shows an equivalent circuit of analog input. A diode is connected to pins for ESD protection.

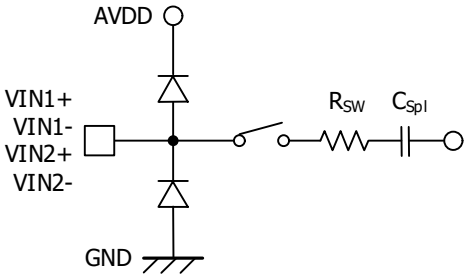


Figure-6. Equivalent analog input circuit

Data format

The data output from SDO1 and SDO2 is in two's complement binary format.

Table-1 shows analog input voltage and ideal output codes.

Table-1. Differential analog input voltage and ideal output codes (note[10])

State	Input voltage		Pseudo differential input voltage (VIN*+) - (VIN*-)	Output code (note[11])	
	VIN*-	VIN*+		BIN	HEX
+Full scale	VREF*	2 × VREF* - 1 LSB	VREF* - 1 LSB	0111 1111 1111 1111	7FFF
Middle scale		VREF*	0	0000 0000 0000 0000	0000
Middle scale - 1 LSB		VREF* - 1 LSB	-1 LSB	1111 1111 1111 1111	FFFF
1 LSB		1 LSB	-VREF* + 1 LSB	1000 0000 0000 0001	8001
-Full scale		0	-VREF*	1000 0000 0000 0000	8000

note[10] : VIN*+, VIN*- and VREF* denotes the following, respectively.
VIN*+ = VIN1+ or VIN2+
VIN*- = VIN1- or VIN2-
VREF* = VREF1 or VREF2

note[11] : The notation is the output code for MM4027A16.
The output code for MM4027A14 and MM4027A12 (+Full scale to Middle scale to -Full scale, HEX) is as follows.
MM4027A14 : 1FFF to 0000 to 2000
MM4027A12 : 7FF to 000 to 800

TYPICAL APPLICATION CIRCUIT

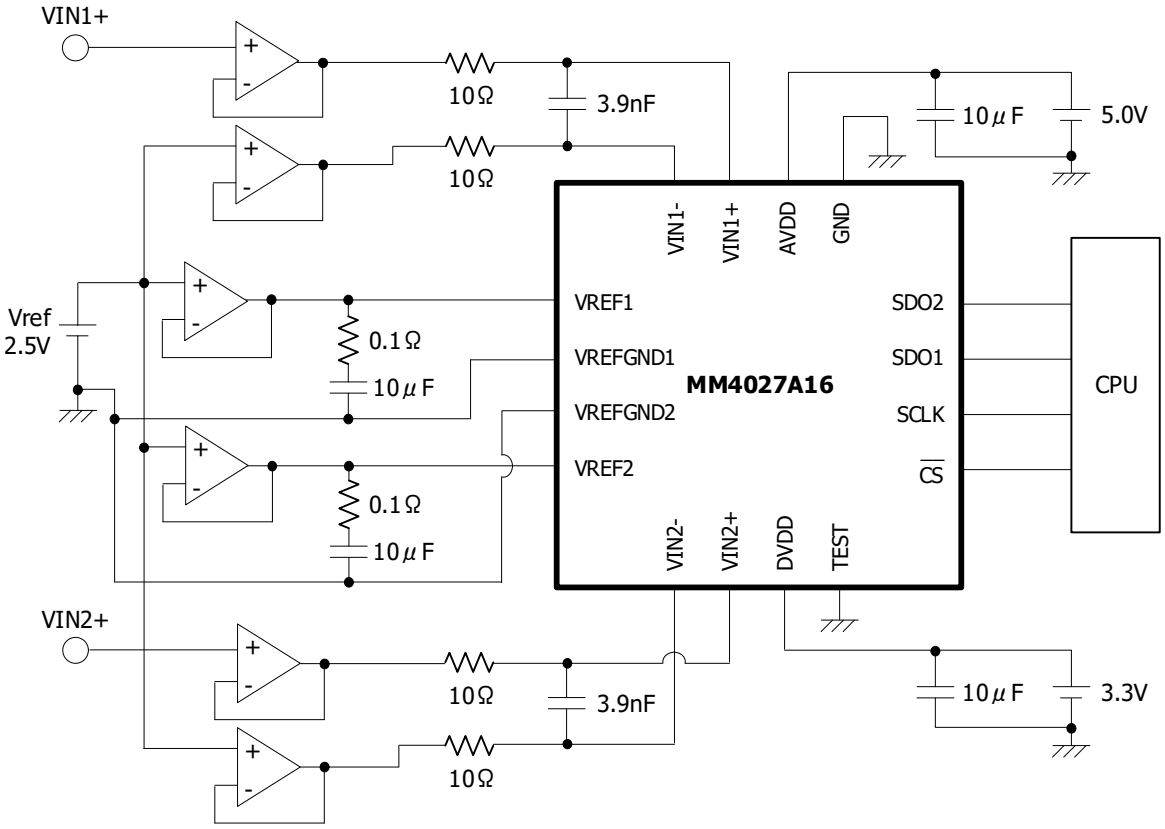


Figure-7. Typical application circuit for 10KHz input signal at 750Ksps

APPLICATION HINTS

- A 10μF ceramic capacitor must be connected near AVDD and DVDD, respectively. This improves voltage ripple and resistance to external noises, and stabilizes the system.

- VREF1 and VREFGND1 pins must be separated from VREF2 and VREFGND2 pins.
  A resistor of 0.1Ω must be connected to the 10μF ceramic capacitor in series near and between VREF1 and VREFGND1 and between VREF2 and VREFGND2 for stabilization.

- High frequency components must be removed from signals input to the analog input pin using an RC low-pass filter. The capacitor not only removes high frequency components from input signals but also reduces the sampling charge injection of the sampling capacitor in ADC. It is recommended that the filter constant be verified with the actual device.

- AVDD, DVDD, GND, VREFGND1, and VREFGND2 wires must be sufficiently strengthened because they may cause noises and unstable operations when their impedance is high.

- AVDD and GND pins and DVDD and TEST pins are positioned side by side, respectively. If short circuit occurs during board mounting, peripheral devices may be destroyed.

TYPICAL PERFORMANCE CHARACTERISTICS

MM4027A16

TBD

TYPICAL PERFORMANCE CHARACTERISTICS

MM4027A14

TBD

TYPICAL PERFORMANCE CHARACTERISTICS

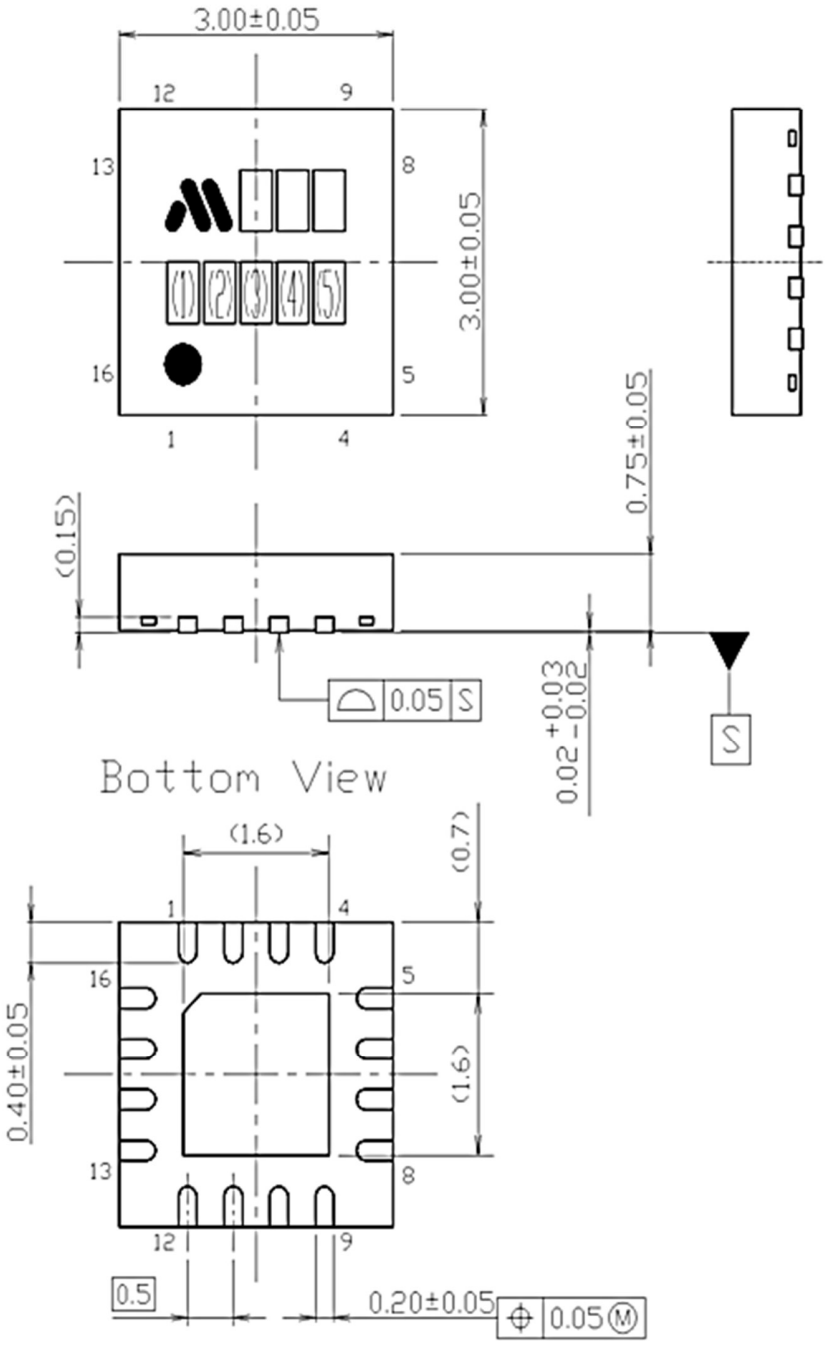
MM4027A12

TBD

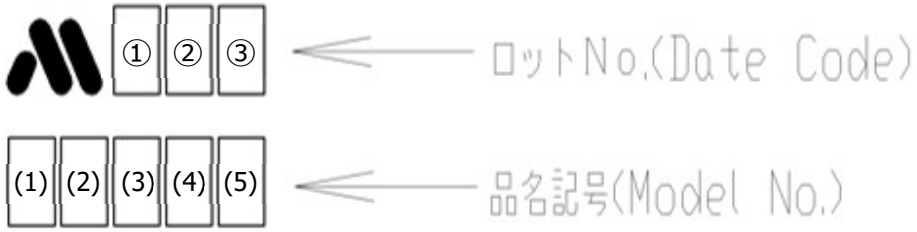
DIMENSIONS

パッケージ:SQFN-16A
PACKAGE

UNIT	mm



MARKING CONTENTS



機種名 Model name	品名記号 Model No.				
	(1)	(2)	(3)	(4)	(5)
TBD			TBD		

【生産年の表記方法/How to indicate a production year】

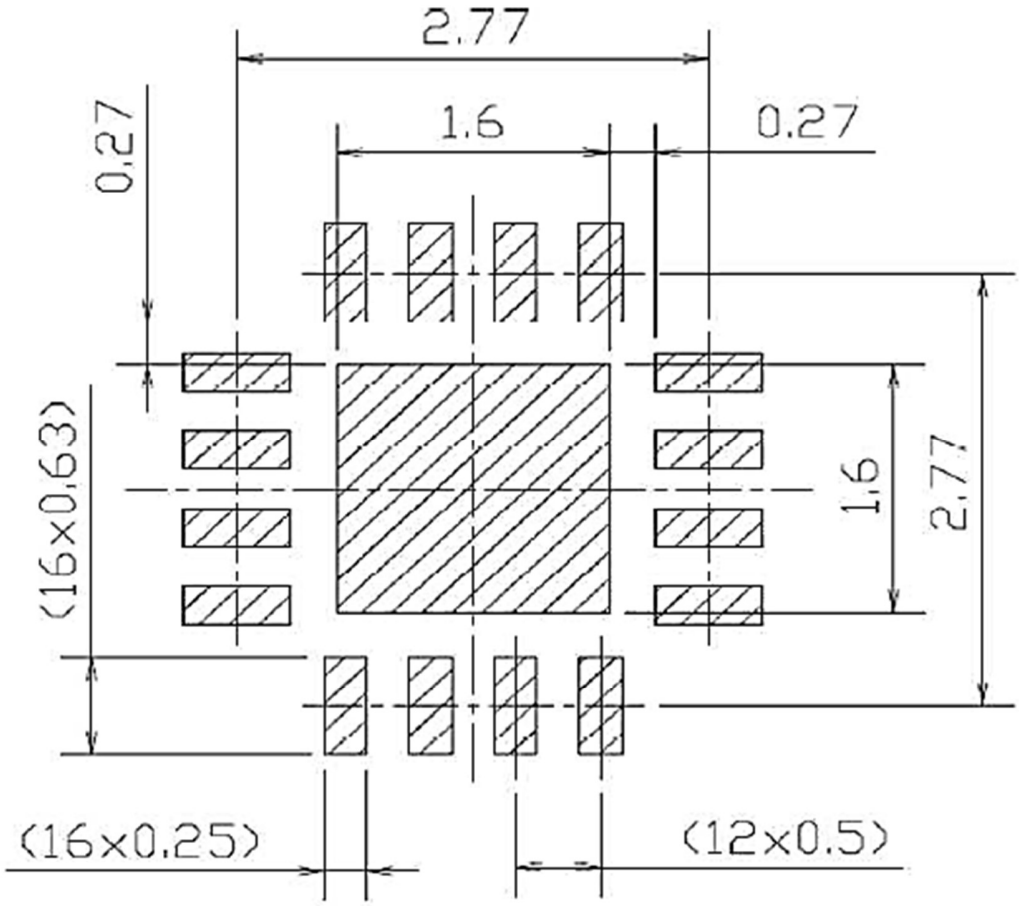
1桁目(①)/The 1st digit (①)	
西暦年末尾 the last digit of a production year	使用表示文字 mark
xxx1	1
xxx2	2
xxx3	3
xxx4	4
xxx5	5
xxx6	6
xxx7	7
xxx8	8
xxx9	9
xxx0	0

2桁目、及び3桁目(②③)/The 2nd and 3rd digit (②③)			
生産週 production week	使用表示文字 mark	生産週 production week	使用表示文字 mark
1	01	27	27
2	02	28	28
3	03	29	29
4	04	30	30
5	05	31	31
6	06	32	32
7	07	33	33
8	08	34	34
9	09	35	35
10	10	36	36
11	11	37	37
12	12	38	38
13	13	39	39
14	14	40	40
15	15	41	41
16	16	42	42
17	17	43	43
18	18	44	44
19	19	45	45
20	20	46	46
21	21	47	47
22	22	48	48
23	23	49	49
24	24	50	50
25	25	51	51
26	26	52	52
		53	53

RECOMMENDED LAND PATTERN

パッケージ:SQFN-16A
PACKAGE

UNIT	mm

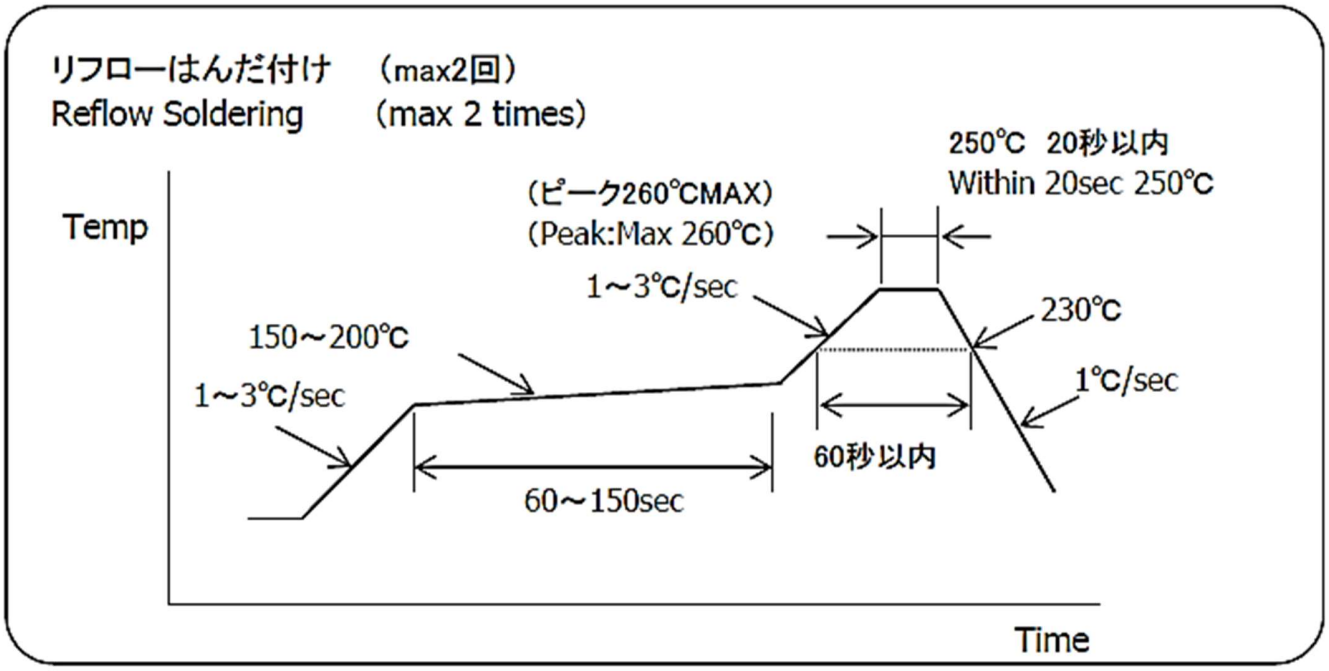


The dimension are for reference only and not guaranteed by design.

To design practically, correction should be made for optimized dimensions considering the effects of the board type to be mounted, mount (soldering) method, type and coating thickness of cream solder.

CONDITION FOR PACKAGE MOUNTING

Pb-Free recommended profile condition



This profile gives recommended values, which are not guaranteed.
For mounting the package, evaluate the profile with the equipment, conditions, and materials to be used.

・Mounting by flow soldering
Flow soldering cannot be used for mounting of this package.

・Mounting by manual soldering
Manual soldering cannot be used for mounting of this package.

CONDITION FOR PACKAGE MOUNTING

Storage method

【Storage condition】

Store the device under the following conditions.

Temperature：5 to 30℃
Humidity：40 to 70%RH
Storage life：1 year

For the product in the moisture-proof packaging, follow these conditions after unpacking.

Temperature：5 to 30℃
Humidity：40 to 70%RH
Storage life：168 hours

Do not store this device where a large amount of dust or harmful volatile gas exists, electrostatic is easily charged, condensation is generated, or changes in temperature and humidity are wide, or under the direct sunlight.

【Baking】

If the storage time specified above has passed, mounting by soldering may cause cracks on the moisture absorbed package. Before mounting, the package should be baked under the following conditions.

Temperature：125℃
Treating time：16 to 24 hours

Embossing tapes and reels are not heat-resistant type.
Before baking, the device should be placed in a heat-resistant container.
In consideration of the time-consuming baking process and the possibility of deformed terminal, the device should be mounted promptly within the time observing the storage conditions.
If a long-term storage is needed, a desiccator or a dry box should be used.

【Handling instructions】

Shipping boxes must be handled with care because any drop or shock may damage the device.
Additionally, the device must be handled in the place with the protection against electrostatic charge and without extreme changes of temperature/humidity.

LINE-UP

Rank	Resolution	Sampling rate	Max. INL	SNR	THD	Status
A16	16-bit	750 ksps	±2.5 LSB	85 dB	-96 dB	Under Planning
A14	14-bit	750 ksps	±1.5 LSB	81.5 dB	-90 dB	Under Planning
A12	12-bit	750 ksps	±1.5 LSB	73 dB	-90 dB	Under Planning

NOTES

Safety Precautions

- Though Mitsumi Electric Co., Ltd. (hereinafter referred to as "Mitsumi") works continually to improve our product's quality and reliability, semiconductor products may generally malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of this product could cause loss of human life, bodily injury, or damage to property, including data loss or corruption. Before customers use this product, create designs including this product, or incorporate this product into their own applications, customers must also refer to and comply with (a) the latest versions or all of our relevant information, including without limitation, product specifications, data sheets and application notes for this product and (b) the user's manual, handling instructions or all relevant information for any products which is to be used, or combined with this products. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. Mitsumi assumes no liability for customers' product design or applications.
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- This product is not designed as a component of equipment or devices that require a high degree of reliability, may affect the life or body, or could damage the property (space systems, submarine repeaters, nuclear power controllers, infrastructure controllers, medical equipment, military devices, units related to the control and safety of transport equipment (automobiles, trains, aircraft, etc.), traffic signaling equipment, disaster / crime prevention units, or the like). In the case where this product is used in these applications, Mitsumi does not bear any responsibility. If the product is used as a component of the above equipment or devices, Mitsumi shall not be liable for any damage caused thereby. It is the customer's responsibility to carry out the necessary safety design for the customer's hardware, software and systems.
- Before using this product, even when it is not used for the applications written previous paragraph, notify and present us beforehand if special care and attention are needed for its application, intended purpose, environment of usage, risk, and the design or inspection specification corresponding to them.
- If any damage to our customer is objectively identified to be caused by the defect of this product, Mitsumi is responsible for it. In this case, Mitsumi is liable for the cost limited to the delivery price of this product.

Application considerations during actual circuit design

- The outline of parameters described herein has been chosen as an explanation of the standard parameters and performance of the product. When you actually plan to use the product, please ensure that the outside conditions are reflected in the actual circuit and assembling designs.
- Before using this product, please evaluate and confirm the actual application with this product mounted and embedded.
- To investigate the influence by applied transient load or external noise, It is necessary to evaluate and confirm them with mounting this product to the actual application.
- Any usage above the maximum rating may destroy this product or shorten the lifetime. Be sure to use this product under the maximum rating.
- If you continue to use this product highly-loaded (applying high temperature, large current or high voltage; or variation of temperature) even under the absolute maximum rating and even in the operating range, the reliability of this product may decrease significantly. Please design appropriate reliability in consideration of power dissipation and voltage corresponding to the temperature and designed lifetime after confirming our individual reliability documents (such as reliability test report or estimated failure rate). It is recommended that, before using this product, you appropriately derate the maximum power dissipation (typically, 80% or less of the maximum value) considering parameters including ambient temperature, input voltage, and output current.

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  - Environment with strong static electricity or electromagnetic wave
  - Environment with high temperature or high humidity where dew condensation may occur
- This product is not designed to withstand radioactivity, and must avoid using in a radioactive environment.

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Strategy Engineering Department Semiconductor Business Division
Tel: +81-46-230-3470 / https://product.minebeamitsumi.com/en/contact/

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